ABSTRACT OF THE DISCLOSURE

A CMOS-logic compliant output buffer design for clock signals which limits the output amplitude without shifting the DC cross point while preserving the duty cycle. The waveform's VOH is limited to a VOHmax value less than VDD and its VOL is limited to a VOLmin value grater than 0V. For charging, the output buffer circuit is open but the current is limited to charging the capacitive load to VOHmax which is less than VDD and the output buffer circuit is tri-stated when VOH reaches VOHmax. For discharging, the output buffer circuit is open, but the current is limited to discharging the capacitive load to VOLmin which is greater than 0V and the output buffer circuit is tri-stated when VOL reaches VOLmin. In this way, the signal amplitude and current consumption are reduced while maintaining sharp rising and falling edges as well as preserving the duty cycle.